60. A system of viewing video information stored on a removable high capacity storage medium, the system comprising:

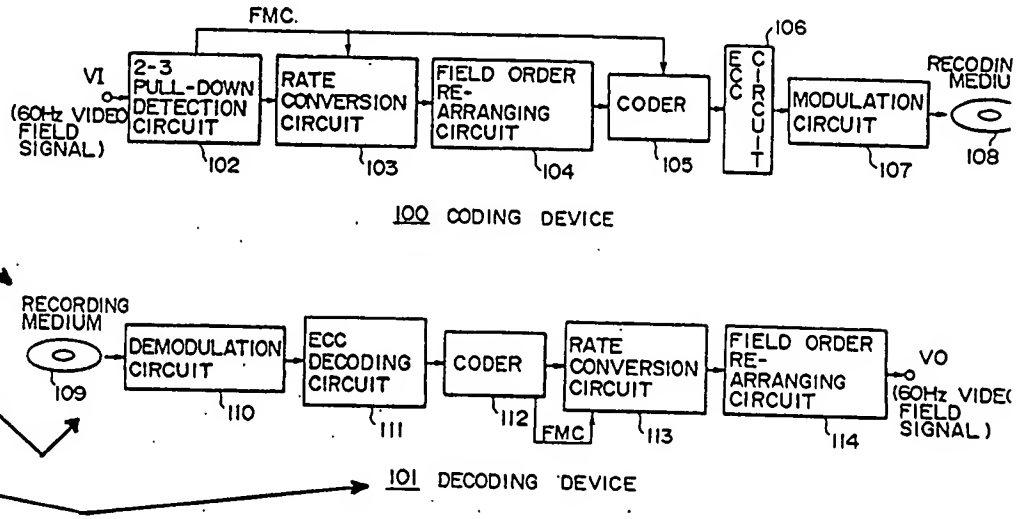
an input device configured to read the video information from the high capacity storage medium, the video information stored on the high capacity storage medium having a digital audio component and a digital video component, the digital video component having an intermediate format having a frame rate of substantially 24 frames per se fps),

the digital video component having been formed by converting input video information having an input format with no added redundant frames or fields;

a graphics processor in data communication with the input device and configured to convert the digital video component in its intermediate format to output video information in an output format, the output format having a frame rate that is greater than or equal to the frame rate of the intermediate format, the graphics processor further being capable of being in data communication with a display device for viewing the output video information in the output format.

*not a structural limitation

FIG. 3



The field order re-arrangement circuit **104** converts the signal from the rate conversion circuit **103** into a progressive (non-interlaced) picture signal having a frame-rate of 24 Hz. The encoder **105** then compresses and codes the picture signal, and feeds the result to the ECC circuit **106**, which adds error correction codes. The modulation circuit **107** modulates the signal from the ECC circuit for recording on the recording medium **108**.

The decoding apparatus **101** receives the signal reproduced from the recording medium **109**. The recording medium **109** is the same as, or is derived from, the recording medium **108** on which the signal generated by the coding apparatus **100** is recorded. The reproduced signal is demodulated by the demodulation circuit **110**, and fed to the ECC decoding circuit **111**, where error detection and correction is applied. The decoder **112** decodes the signal from the ECC decoding circuit into pictures with a frame rate of 24 Hz. The rate conversion circuit **113** converts the picture signal with a frame rate of 24 Hz into a video signal with a field rate of 60 Hz. The field order re-arrangement circuit **114** returns the field order of the video signal with a 60 Hz field rate from the decoder **112** to that of the coder input signal VI, and provides the decoder apparatus output signal VO with a field rate of 60 Hz.